SAT in Logic Synthesis

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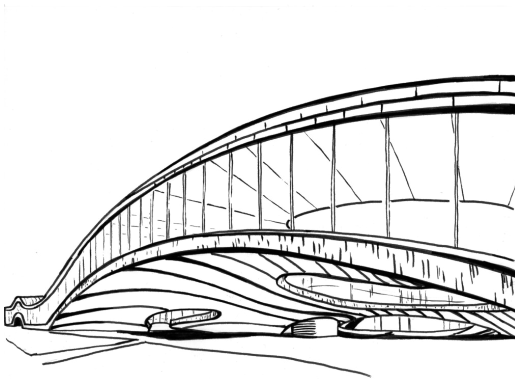
EPFL



Background

SAT-based area recovery in structural technology mapping

Applying logic synthesis to speedup SAT

SAT-based exact synthesis: encodings, topology families, and parallelism

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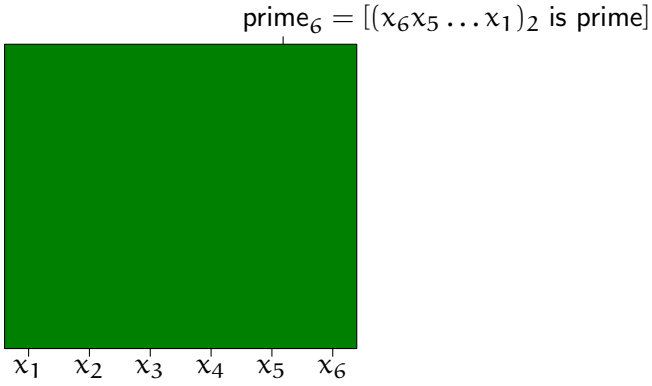
Decompose large functions using k-LUT mapping



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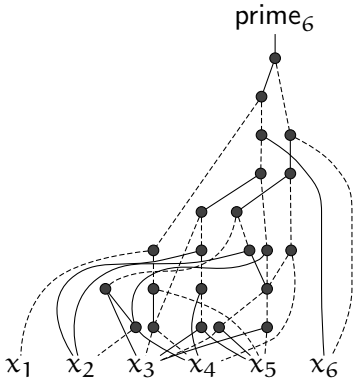

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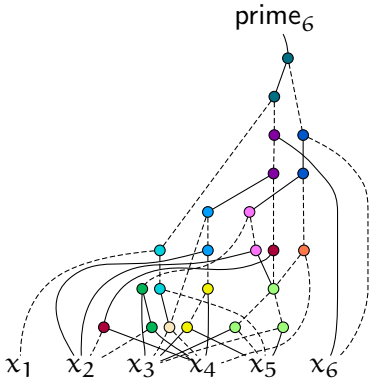

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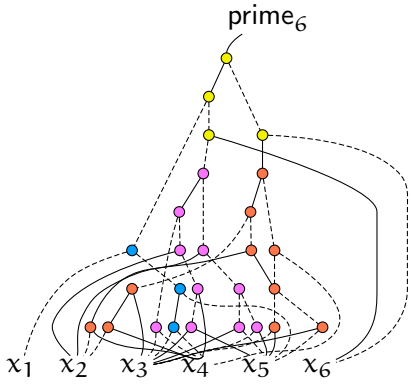

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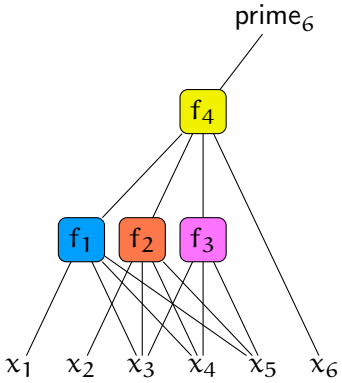

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2. Cover network with subnetworks with limited fanin size k (here $k = 3$ and $k = 4$)
3. Collapse covered subnetworks into lookup-table nodes

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[B. Schmitt, A. Mishchenko, and R.K. Brayton, *ASP-DAC* 23 (2018), 586–591]

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- How to make it reliably efficient for large networks?

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- $\sum m_i \leqslant L$

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- Find good pivots to extract windows
- Cache windows to avoid duplicate optimization effort

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Implementation

ABC

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- Not fully finished (PR #122)

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- Disadvantage: Requires the use of many auxiliary variables

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- Cost function based on CNF size
- May even lead to fewer number of overall clauses

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[W. Haaswijk, M. Soeken, A. Mishchenko, and G. De Micheli, SAT-Based Exact Synthesis: Encodings, Topology Families, and Parallelism *TCAD*, to appear]

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