

Quo vadis, Logic Synthesis

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Outline

- 1 A retrospective: 35 years after the Espresso book
- 2 Twenty-seven challenges from twenty years ago

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Logic Synthesis in Retrospective

- Underlying mathematics: Boolean algebra for combinational logic and Automata theory for sequential logic
- Techniques for optimization of digital logic design investigated since the 50s
- First theoretical result: exact minimization of Sum of Products with the procedure of Quine-McCluskey
- Intense research published by IRE Transactions on Computers, then IEEE Transactions on Computers (later on this role was partly played by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems)

The Birth of Computer-Aided IC Design

- Academic and industrial research gives birth in the 70s to design automation of integrated circuits
- UCB plays a key role, first with a sustained research effort to produce SPICE, a program to simulate electronic circuits, by advanced numerical analysis techniques
- IC and computer industry give a key contribution, e.g., a leading center was IBM's T.J.Watson Research Center in Yorktown Heights; design automation is developed internally by major companies to provide tools for own designers. Similar developments in Japan, e.g., at Fujitsu

Everything Happened in the Eighties

- Academic and industrial research covers more steps of design automation besides simulation: from physical design to data base infrastructure
- A collaboration between UCB and IBM ushers into the phase of modern logic synthesis targeting tools that handle industrial problems
- Mead and Conway popularize structured IC design as an exercise for computer science students (VLSI literacy for all ?)
- People from industry and academia start the industry of CAD vendors to enable IC design for a larger basis of industrial customers (Mentor Graphics, 1981, now a Siemens Business; Synopsys, 1986; Cadence Design Systems, by mergings, 1988, etc.)

The Birth of Modern Logic Synthesis

- In 1984, Robert Brayton (IBM Yorktown, then UCB), Gary Hachtel (UCB, Colorado at Boulder), Curt McMullen (Harvard U., recipient of the Fields Medal in 1998) and A. Sangiovanni-Vincentelli (UCB) wrote the Espresso book: **Logic minimization algorithms for VLSI synthesis, Kluwer, 1984 (now Springer)**
Google Scholars citations: 2096
- The book introduced a number of key ideas in logic synthesis: the unate recursive paradigm based on cofactoring until unate leaves, for basic computations like primes, complement, tautology; exact and heuristic based on iteration of reduce, expand, irredundant, etc.

Espresso Again

- In 1987, R. Rudell (UCB) and A. Sangiovanni-Vincentelli (UCB), published the definitive Espresso paper:
Multiple-valued minimization for PLA optimization, IEEE Trans. on CAD of IC and Systems, Vol. 6, n. 5 , Sep. 1987
Google Scholar citations: 472

The paper generalized the ideas of the Espresso book to multiple-valued input logic, cast multi-output minimization as multi-valued input minimization (from a result due to T. Sasao), extended Shannon cofactoring and monotonicity (weak form) to multi-valued logic

- Rudell made also available the Espresso package, featuring a large collections of commands to manipulate and optimize the two-level representation of Boolean functions

Applications of Espresso MV

- FSM encoding (the KISS paper) modeled as MV input encoding (Espresso book formulates input encoding as MV minimization, KISS paper describes the first exact algorithm to satisfy input encoding constraints):
G. De Micheli, R. Brayton, A. Sangiovanni-Vincentelli, Optimal state assignment for finite state machines, IEEE Trans. on CAD of ICs and Systems, 1985
Google Scholars citations: 400
- FSM encoding (the NOVA paper) modeled as MV input (and partially MV output) encoding:
T. Villa, A. Sangiovanni-Vincentelli, NOVA: state assignment of finite state machines for optimal two-level logic implementation, IEEE Trans. on CAD of ICs and Systems, 1990
Google Scholars citations: 451

Was Espresso the End of it ?

- In 1993, J. Sanghavi, P. McGeer, R. Brayton, and A. Sangiovanni-Vincentelli improved Espresso exact:
ESPRESSO-SIGNATURE: a new exact minimizer for logic functions. IEEE Trans. VLSI Syst. 1(4): 432-440 (1993)
- The idea is to derive the covering problem directly and implicitly without generating the set of all prime implicants, but only those prime implicants involved in the covering problem
- A set of primes is represented by the cube of their intersection; the unique set of sets of primes that forms the covering problem can be implicitly represented by a set of cubes that forms a minimum canonical cover

Was Espresso the End of it ? BDDs ...

- In 1992, Coudert and Madre from France published:
Implicit and incremental computation of primes and essential primes of Boolean functions
Google Scholars citations: 216
- In 1993, G. Swamy, R. Geer and R. Brayton at UCB published:
A fully Quine-McCluskey procedure using BDDs, Proc. IWLS 1993
- Both teams applied BDDs to represent primes, the minterm-prime covering table and its reduction process

Was Espresso the End of it ? BDDs/ZDDs

- In 1993-95, O. Coudert, J.-C. Madre, and H. Fraisse developed further the exact implicit computation. We refer to the papers by O. Coudert:
Two-Level Logic Minimization: an Overview, Integration, vol. 15, n. 2, p. 97-140, Oct. 1994.
Google Scholars citations: 235
Doing Two-Level Logic Minimization 100 Times Faster, Proc. of SODA, June 1995
- They introduced a BDD/ZDD-based implicit cyclic core computation based on the notion of transposing functions
- The authors produced the program SCHERZO (developed with the TiGeR library) for exact implicit/explicit two-level minimization

MIS: Multi-Level Logic Synthesis

- Two-level synthesis was mapped to PLAs, and similar array logic
- More flexible architectures (standard cells, etc.) motivated working on synthesis of multi-level logic
- In 1987, building on the notion of Boolean network (an acyclic graph whose nodes were PLAs), R. Brayton, R. Rudell, A. Sangiovanni-Vincentelli, and A. Wang, built the theory of combinational multi-level logic optimization

MIS: A multiple-level logic optimization system, IEEE Trans. on CAD of IC and Systems, Vol. 6, n. 6, Nov. 1987
Google Scholars citations: 1366

MIS: Multi-Level Logic Synthesis

- The package MIS was based on a set of operations for restructuring and simplification with algebraic divisors (kernels) and Boolean divisors
- Some operations: decomposition (single functions), extraction (multiple functions), factoring (series-parallel decomposition), substitution, collapsing (aka elimination), simplification
- Commands organized in heuristic scripts, trading-off quality vs. computation time, for area and/or delay
- An extensive reference by R. Brayton, G. Hachtel, A. Sangiovanni-Vincentelli is:
Multilevel logic synthesis, Proceedings of the IEEE 78 (2), 264-300, Feb. 1990
Google Scholars citations: 506

The Complexity of Logic Minimization

- SOP minimization is NP-complete from truth tables and Σ_2^P -complete from SOPs (and many other problems in two-level minimization)
C. Umans, T. Villa, A. Sangiovanni-Vincentelli, Complexity of two-level logic minimization, IEEE Trans. on CAD of ICs and Systems, 2006
- Given a Boolean circuit, find the smallest Boolean circuit that computes the same function (Minimum Equivalent Expression). The input and output circuit may be required to be circuits of a particular form, e.g., Boolean formulas, or bounded-depth circuits. It is Σ_2^P -complete for depth- k formulas for $k \geq 2$, and for unbounded-depth formulas
D. Buchfuhrer, C. Umans, The complexity of Boolean formula minimization, Journal of Computer and System Sciences, 2011

SIS: Sequential Multi-Level Synthesis

- Faculty: R. Brayton and A. Sangiovanni-Vincentelli
- Main architects: Ellen Sentovich and Kanwar Jit Singh
- Contributors: Srinivas Devadas (MUSTANG program), Bill Lin (JEDI program), Luciano Lavagno, Sharad Malik, Cho Moon, Rajeev Murgai, Alex Saldanha, Hamid Savoj, Narendra Shenoy, Tom Shiple, Paul Stephan, Colin Stevens, Herve Touati, Tiziano Villa (NOVA program), and Carol Wawrukiewicz. Jose Monteiro (MIT) contributed the power estimation package. David Long (AT&T Bell Laboratories) contributed the BDD package. June Rho (CU Boulder) contributed the STAMINA program.
- Richard Rudell and Albert Wang had written the program MISII, upon which SIS is built.

SIS: Sequential Multi-Level Synthesis

- SIS upgraded MIS to sequential logic synthesis, pairing a Boolean network with a corresponding Finite State Machine, and converting from the behavioral (FSM) to the structural view and back with the synthesis/extract transformations
- Restructuring was extended to networks with gates and memory elements (e.g., retiming)
- State minimization and state assignment were introduced respectively to minimize the states and to convert an FSM into a sequential network

SIS: A system for sequential circuit synthesis, EECS Department, University of California, Berkeley Technical Report No. UCB/ERL M92/41 1992
Google Scholars citations: 1990

VIS: Verification and Synthesis

- Faculty: R. Brayton, G. Hachtel, A. Sangiovanni-Vincentelli and F. Somenzi
- Main architects: Thomas Shiple
- Contributors: Adnan Aziz, Szu-Tsung Cheng, Stephen Edwards, Adrian Isles, Sunil Khatri, Yuji Kukimoto, Abelardo Pardo, Shaz Qadeer, Rajeev K. Ranjan, Sriram Rajamani, Shaker Sarwary, Thomas R. Shiple, Gitanjali Swamy, Serdar Tasiran, Tiziano Villa

VIS: Verification and Synthesis

- VIS (Verification Interacting with Synthesis) integrates the verification, simulation, and synthesis of finite-state hardware systems. It uses a Verilog front end and supports fair CTL model checking, language emptiness checking, combinational and sequential equivalence checking, cycle-based simulation, and hierarchical synthesis.

Main publication:

VIS: A System for verification and Synthesis, CAV 1996

Google Scholars citations: 890

- Influenced by joint work with R. Kurshan (ATT) on ω -regular finite automata (L-automata), see the tool COSPAN and Robert Kurshan Computer-Aided Verification of Coordinating Processes - The Automata-Theoretic Approach, Princeton University Press, 1995

Multi-Valued Multi-Level Synthesis

- The next big effort by Brayton's group was to develop MVSIS, a program to optimize multi-valued multi-level networks (MV networks)
- MVSIS is modeled after SIS, but in the logic network of MVSIS all variables can be multi-valued each with its own range. Included in MVSIS are almost all the technology-independent transformations of SIS, as well as transformations specific to multi-valued nodes such as merge, pair decode, encode.

M. Gao, J.-H. Jiang, Y. Jiang, Y. Li, A. Mishchenko, S. Sinha, T. Villa, R. Brayton, Optimization of multi-valued multi-level networks, Proc. of the 32th Int. Symp. on Multiple-Valued Logic, Boston, May 2002
Google Scholar citations: 33

BALM and BALM-II

- Originally an offspring of MVSIS (MVSIS 3.0) and developed at Berkeley by A. Mishchenko, T. Villa and R. Brayton in 2004-2005, BALM (Berkeley Automata and Language Manipulation) aims at providing an experimental environment for efficient manipulation of finite automata in various application domains, e.g., synthesis, verification, control, etc.
- Given a network of FSMs with known components (context) and unknown ones, BALM was motivated to implement the computation of the unknown component, formulating the problem as solving an equation over regular languages

BALM and BALM-II

- The theory behind the tool is presented in
T. Villa, N. Yevtushenko, R. Brayton, A. Mishchenko A. Petrenko, The unknown component problem: theory and applications, Springer 2011
T. Villa, A. Petrenko, N. Yevtushenko, A. Mishchenko, R. Brayton, Component-based design by solving language equations, Proceedings of the IEEE 103 (11), 2152-2167, 2015
- The applicability of BALM to finite-state machine synthesis was demonstrated by solving an unknown component problem in sequential synthesis formulated using language equations
- Effectiveness and efficiency still open problems !

BALM and BALM-II

- BALM-II is an extension of BALM developed in 2012 at the University of Verona (G. Castagnetti, M. Piccolo, T. Villa) to support interleaving composition (BALM supports only synchronous composition)
- BALM-II (which subsumes BALM) available at <https://jackhack96.github.io/logic-synthesis/balm.html#overview>
G. Castagnetti, M. Piccolo, T. Villa, N. Yevtushenko, A. Mishchenko, R. Brayton, Solving Parallel Equations with BALM-II, Technical Report No UCB/EECS-2012-181, EECS, UCB, 2012
- At the same site, the legacy code of ESPRESSO, SIS and MVSIS is available
<https://jackhack96.github.io/logic-synthesis/>

ABC

- Last and current major effort in logic synthesis and verification by the UCB school: ABC, by Alan Mishchenko and Robert Brayton
- ABC is a tool for logic synthesis and formal verification of binary logic circuits appearing in synchronous hardware designs. ABC combines scalable logic transformations based on And-Inverter Graphs (AIGs), with a variety of innovative algorithms. The synergy of sequential synthesis and sequential verification improves both.

R. Brayton and A. Mishchenko, ABC: An Academic Industrial-Strength Verification Tool, Proc. CAV'10, Springer, LNCS 6174, pp. 24-40
Google Scholars citations: 429

EPFL LS Libraries and Benchmarks

- The EPFL logic synthesis libraries are a collection of modular open source C++ libraries for the development of logic synthesis applications. They can be readily used as core components in complex logic synthesis frameworks.
M. Soeken, H. Riener, W. Haaswijk, and G. De Micheli, The EPFL Logic Synthesis Libraries, IWLS 2018, pre-print available at [arXiv:1805.05121](https://arxiv.org/abs/1805.05121)
- The EPFL Combinational Benchmark Suite was introduced in 2015 with the aim of defining a new comparative standard for the logic optimization and synthesis community. The benchmark suite is divided into arithmetic, random/control and MtM circuits, and each circuit is distributed in Verilog, VHDL, BLIF and AIGER formats.

The Love Story of EDA with BDDs

- In 1985, R. Bryant presented at DAC a new canonical data structure and manipulation algorithms for representing Boolean functions by directed acyclic graphs.

R. Bryant, Graph-based algorithms for Boolean function manipulation, IEEE Trans. on Comp., C-35-8, pp. 677-691, Aug. 1986

Google Scholars citations: 11167

R. Bryant, Symbolic Boolean manipulation with ordered binary-decision diagrams, ACM Computing Surveys (CSUR) 24 (3), 293-318, 1992

Google Scholars citations: 2749

K. Brace, R. Rudell, R. Bryant, Efficient implementation of a BDD package, ACM/IEEE Proc. 27th DAC, 40-45, 1990

Google Scholars citations: 1655

R. Bryant, On the complexity of VLSI implementations and graph representations of Boolean functions with application to integer multiplication, IEEE Trans. on Comp. 40 (2), 205-213

Google Scholars citations: 669

Specialized Conferences: IWLS

- IWLS (International Workshop on Logic Synthesis, from 2001 International Workshop on Logic and Synthesis) started in 1987
- In Nov. 2000 the TPC of IWLS, while organizing the 10th International Workshop on Logic & Synthesis to be held in June 12-15, 2001 (Granlibakken, Lake Tahoe, California), decided to celebrate with a book, published in 2002, as (eds.) S. Hassoun, T. Sasao, R. Brayton, *Logic Synthesis and Verification*, Kluwer 2002 (now Springer)
- Today, we are at the 28th International Workshop on Logic & Synthesis, June 21-23, 2019, EPFL, Lausanne, Switzerland

Specialized Conferences: IWBP

- IWBP (International Workshop on Boolean Problems), held every two years, previous editions until the 12th in Freiberg (Saxony, Germany) always organized by its founder, Prof. Berndt Steinbach
- Last edition (13th International Workshop on Boolean Problems, IWSBP) in 2018, Bremen (Germany), organized by Prof. Rolf Drechsler
- In the past, large participation of researchers from former Soviet Union and Eastern Europe, which originally contributed to put in contact these communities
- Selection of best papers published in book collection after the workshop

Tools of the Trade

- G. De Micheli, Synthesis and optimization of digital circuits, McGraw-Hill Higher Education, 1994
- G. Hachtel, F. Somenzi, Logic synthesis and verification algorithms, Kluwer 1996, (now Springer)
- S. Devadas, A. Ghosh, K. Keutzer, Logic synthesis, McGraw-Hill, 1994
- (Eds.) Y. Crama and P. Hammer, Boolean functions: Theory, algorithms, and applications, Encyclopedia of Mathematics and its Applications 142, Cambridge U.P., 2011
- (Eds.) Y. Crama and P. Hammer, Boolean models and methods in mathematics, computer science, and engineering, Encyclopedia of Mathematics and its Applications 134, Cambridge U.P., 2010

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The Future of Logic Synthesis in 2002

Revisiting the agenda suggested by Bob Brayton 20 years ago:

- Techniques on the edge
- Physical/Logical design
- DSM issues/Design for Low power
- Use in software compilers
- Sequential issues
- Efficient representations of logic functions/BDDs
- Minimum implementations of logic functions
- Static timing analysis
- SAT and ATPG
- Equivalence checking

Ready for the Technical Talks

- In the talks of the workshop we will get contemporary points-of-view addressing and implicitly answering to some of the challenges posed by Brayton
- Majority of the talks focused on combination logic (we could not cover everything, decided to go for depth over breadth)
- An analytical comparison of the concerns of twenty years ago and now is the matter for another talk

Grazie per l'attenzione !

Thanks for your attention !